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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,718	09/30/2003	Robert A. Corley	2	6317

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Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

EXAMINER	
RIYAMI, ABDULLA A	

ART UNIT	PAPER NUMBER
2616	

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03/18/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/675,718	CORLEY, ROBERT A.	
	Examiner	Art Unit	
	ABDULLAH RIYAMI	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is in response to an amendment/response filed on 01/30/2008. Claims 1, 6, 10, 11, 15, 19, and 20 have been amended. No claims have been added. No claims have been canceled. Claims 1-20 remain pending in the application.

Claim Rejections - 35 USC § 103

1. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.

2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park et al. (5872770).

As per claim 1, Park et al. discloses a processor (see figure 1, block 30) comprising: controller circuitry operative to control performance of a continuity check for each of a plurality of flows of protocol data units received by the processor (see figure 3, column 9, lines 1-22) and memory circuitry stores an identifier for each of a subset of the plurality of flows (see column 9, lines 1-12); wherein the controller circuitry controls access to a set of continuity check counters comprising a counter for each of the plurality of flows (see figure 3, block 32); the controller circuitry determining if a given flow for which a protocol data unit is received in the processor has a corresponding entry in the continuity check memory (see column 9, lines 23-35), and if the given flow has such an entry, preventing a corresponding one of the continuity check counters from being updated (see column 9, lines 23-67), and if the given flow does not have such an entry, clearing the corresponding one of the continuity check counters and storing a flow identifier for the given flow in the continuity memory (see column 9, lines 23-67).

Park et al. does not expressly disclose the memory circuitry comprising a continuity check cache.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement continuity memory (see column 9, lines 1-12) also act as fast access continuity cache memory within the same processor.

The motivation to combine would have been to have a dedicated continuity check cell processor having faster and more efficient operation, administration, and maintenance cell processing.

As per claim 2, Park et al. discloses a processor (see figure 1, block 30) wherein the memory circuitry comprises an internal memory of the processor, and the continuity check cache is implemented in its entirety within the internal memory (see figure 1, block 30).

As per claim 3, Park et al. discloses a processor (see figure 1, block 30) wherein the set of continuity check counters are stored in an external memory associated with the processor (can be viewed as external memory, see figure 3, block 32).

As per claim 4, Park et al. discloses a processor (see figure 1, block 30) wherein at least one of the continuity checks is performed in a manner compliant with an I.610 protocol (see column 10, lines 6-8, default value being 3.5 seconds is accordance to ITU-I160 standard.

As per claim 5, Park et al. discloses a processor wherein at least one of the protocol data units comprises a cell (see column 9, lines 1-7).

As per claim 6, Park et al. discloses a processor (see figure 1, block 30) wherein the continuity check cache has a capacity of M entries, a given one of which may

correspond to the flow identifier, and the set of continuity check counters includes N continuity check counters, where M is substantially less than N (see figure 3, block 32).

As per claim 7, Park et al. discloses a processor (see figure 1, block 30) wherein one or more of the flows correspond to particular network connections (see column 9, lines 1-9).

As per claim 8, Park et al. discloses a processor (see figure 1, block 30) wherein each of the flows for which a flow identifier is stored in the continuity check cache has had its corresponding continuity check counter cleared upon receipt of a first protocol data unit for that flow within a specified time window (see column 9, lines 23-35).

As per claim 9, Park et al. discloses a processor (see figure 1, block 30) wherein each of the continuity check counters is configured so as to be incremented if one or more protocol data units are not received for the corresponding flow within a specified time window (see (see column 9, lines 23-35).

As per claim 10, Park et al. discloses a processor (see figure 1, block 30) wherein in conjunction with a continuity check performed for the given flow the continuity check fails and a timeout indication is generated if the corresponding continuity check counter reaches a particular value (see column 9, lines 23-50).

As per claim 11, Park et al. discloses a processor (see figure 1, block 30) wherein in conjunction with a continuity check performed for the given flow a corresponding one of the continuity check counters is reset only a single time for a plurality of protocol data units received by the processor for the given flow within a specified time window (see column 9, lines 1-40).

As per claim 12, Park et al. discloses a processor (see figure 1, block 30) wherein at least one of the continuity check counters comprises a multi-bit counter with each increment of the count representing a specified time window within a designated period of time for which the continuity check is performed (see reference maybe any number, column 10, lines 6-10).

As per claim 13, Park et al. discloses a processor (see figure 1, block 30) wherein at least one of the continuity check counters comprises a three-bit counter with each increment of the count corresponding to a time window having a duration of approximately 0.5 seconds (column 10, lines 6-10).

As per claim 14, Park et al. discloses a processor (see figure 1, block 30) wherein the entries of the continuity check memory are cleared after expiration of each of a plurality of time windows for which the continuity check counters can be incremented (see column 9).

As per claim 16, Park et al. discloses a processor (see figure 1, block 30) wherein the processor is configured to provide an interface for communication of the received protocol data units between a network and a switch fabric (see column 1, lines 6-12).

As per claim 17, Park et al. discloses a processor (see figure 1, block 30) wherein the processor comprises a network processor (see column 1, lines 28-35).

As per claim 18, Park et al. discloses a processor (see figure 1, block 30) wherein the processor is configured as an integrated circuit (see figure 3).

As per claims 2-14 and 16-18, Park et al. does not expressly disclose the memory circuitry comprising a continuity check cache.

As per claims 2-14 and 16-18, at the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement continuity memory (see column 9, lines 1-12) also act as fast access continuity cache memory within the same processor.

As per claims 2-14 and 16-18, the motivation to combine would have been to have a dedicated continuity check cell processor having faster and more efficient operation, administration, and maintenance cell processing.

As per claim 19, Park et al. discloses a method for use in a processor (see figure 1, block 30) comprising controller circuitry operative to control performance of a continuity check for each of a plurality of flows of protocol data units received by the processor (see figure 3, column 9, lines 1-22), the controller circuitry being further operative to control access to a set of continuity check counters comprising a counter for each of the plurality of flows (see column 9, lines 23-35), the method comprising the steps of: storing an identifier for each of a subset of the plurality of flows in a continuity check memory (see column 9, lines 1-12); and determining if a given flow for which a protocol data unit is received in the processor has a corresponding entry in the continuity check memory (see column 9, lines 23-67), and if the given flow has such an entry, preventing a corresponding one of the continuity check counters from being updated, and if the given flow does not have such an entry, clearing the corresponding

one of the continuity check counters and storing a flow identifier for the given flow in the continuity check memory (see column 9, lines 23-67).

Park et al. does not expressly disclose a continuity check cache.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement continuity check memory (see column 9, lines 1-12) also act as fast access continuity cache memory within the same processor.

The motivation to combine would have been to have a dedicated continuity check cell processor having faster and more efficient operation, administration, and maintenance cell processing.

As per claim 20, Park et al. discloses an article of manufacture comprising a computer machine-readable medium having at least one computer program encoded therein for use in a processor (see column 1, lines 22-25) comprising controller circuitry operative to control the performance of a continuity check for each of a plurality of flows of protocol data units received by the processor (see figure 3, column 9, lines 1-22), the controller circuitry being further operative to control access to a set of continuity check counters comprising a counter for each of the plurality of flows (see column 9, lines 23-35), the program code when executed in the processor implementing the steps of: storing an identifier for each of a subset of the plurality of flows in a continuity check memory (see column 9, lines 1-12); and determining if a given flow for which a protocol data unit is received in the processor has a corresponding entry in the continuity check memory (see column 9, lines 23-67), and if the given flow has such an entry, preventing a corresponding one of the continuity check counters from being updated, and if the

given flow does not have such an entry, clearing the corresponding one of the continuity check counters and storing a flow identifier for the given flow in the continuity check memory (see column 9, lines 23-67).

Park et al. does not expressly disclose a continuity check cache.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to implement continuity check memory (see column 9, lines 1-12) also act as fast access continuity cache memory within the same processor.

The motivation to combine would have been to have a dedicated continuity check cell processor having faster and more efficient operation, administration, and maintenance cell processing.

As per claim 15, Park et al. discloses a processor (see figure 1, block 30) but does not expressly disclose if the continuity check cache is full when one of the plurality of flows first arrives at the processor, a particular flow identifier from the cache is removed to make room for storage of a flow identifier for the arriving flow. However, the deletion of an entry from cache memory when full is well known in the art. Thus at the time of the invention, it would have been obvious to a person of ordinary skill in the art, to remove an entry when the cache is full. The motivation to combine would have been to have an efficient continuity check system for operation, administration, and maintenance cell processing.

Response to Arguments

5. Applicant's arguments filed 01/30/2008 have been fully considered but they are not persuasive. Applicant argue that the prior art fails to teach "a set of continuity counters comprises a counter for each of the plurality of flows and a continuity check cache stores an identifier for each of a subset of the plurality of flows. Examiner respectfully disagrees with the characterization of the prior art. Park et al. (5872770) does teach a set of continuity counters comprises a counter for each of the plurality of flows (see figure 3, blocks 32, 35, 31 and 33 and column 9, lines 1-45) and a continuity check cache stores an identifier for each of a subset of the plurality of flows (see figure 3, (each channel is a flow from the plurality of flows) and column 9, lines 1-45).

6. For the reason above, the rejection is maintained.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See form 892.

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH RIYAMI whose telephone number is (571)270-3119. The examiner can normally be reached on Monday through Thursday 8am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Firmin Backer can be reached on (571)272-6703. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Abdullah Riyami/
Examiner, Art Unit 2616

/FIRMIN BACKER/
Supervisory Patent Examiner, Art Unit 2616